II. AMENDMENTS TO THE CLAIMS

The following listing of claims replaces all prior listings, or versions, of claims.

1. (Previously Presented) A method of modeling for use with an integrated circuit (IC) design, the method comprising:

partitioning an edge of a shape in the IC design into a plurality of intervals; and

assigning at least one dimension to each interval;

wherein the partitioning includes:

generating a core Voronoi diagram for the shape, the core Voronoi diagram being generated based on a L∞ metric, the L_∞ metric defining a distance between two points in the shape as the maximum of a horizontal distance and a vertical distance between the two points; and

partitioning the edge based on a core element for each vertex of the core Voronoi diagram, the core element being one of a largest possible core element and a smallest possible core element; and.

wherein in the case that the core element is the largest possible core element, the intervals are as large as possible, and wherein in the case that the core element is the smallest possible core element, the intervals are as small as possible.

2. (Cancelled).

3. (Previously Presented) The method of claim 1, wherein the assigning is based on a Euclidean metric.

4-6. (Cancelled).

7. (Original) The method of claim 1, wherein the at least one dimension includes a width for each interval and a spacing to a neighboring shape for each interval.

8. (Original) The method of claim 1, wherein the dimension is a function of another dimension.

9. (Previously Presented) The method of claim 1, further comprising using the at least one dimension to evaluate a check rule.

10. (Original) The method of claim 9, wherein the check rule involves at least one of: a single edge, a pair of neighboring edges, and edges within more than one layer of the IC design.

11. (Original) The method of claim 1, wherein each concave vertex of the shape is an interval.

12-31. (Cancelled)